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(71) Applicant: **TEXAS INSTRUMENTS
INCORPORATED**
Dallas, TX 75265 (US)

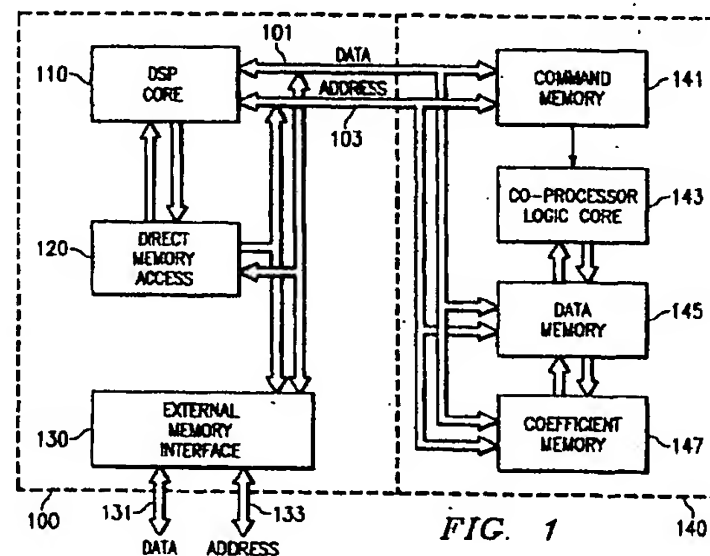
(72) Inventors:
• **Hocevar, Dale E.**
Richardson, Texas 75074 (US)

• **Gatherer, Allan**
Richardson, Texas 75082 (US)
• **Lemons, Karl E. Jr.**
Garland, Texas 75044 (US)
• **Hung, Ching-Yu**
Plano, Texas 75024 (US)

(74) Representative: **Holt, Michael**
Texas Instruments Ltd.,
PO Box 5069
Northampton, Northamptonshire NN4 7ZE (GB)

(54) Data processing system with digital signal processor core and co-processor

(57) A data processing system includes a digital signal processor core (110) and a co-processor (140). The co-processor (140) has a local memory (141, 145, 147) within the address space of the said digital signal processor core (110). The co-processor (140) responds commands from the digital signal processor core (110). A direct memory access circuit (120) autonomously transfers data to and from the local memory (141, 145, 147) of the co-processor (140). Co-processor commands are stored in a command FIFO memory (141) mapped to a predetermined memory address. Control commands includes a receive data synchronism command stalling the co-processor (140) until completion of a memory transfer into the local memory (141, 145, 147). A send data synchronism command causes the co-processor (140) to signal the direct memory access circuit (120) to trigger memory transfer out of the local memory (141, 145, 147). An interrupt command causes the co-processor (140) to interrupt the digital signal processor core (110).



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EUROPEAN SEARCH REPORT

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The present search report has been drawn up for all claims			
Place of search MUNICH		Date of completion of the search 6 May 2002	Examiner Thibaudeau, J
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>			

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